

Krishna Prasad S Rao

MSEE (EMC • Antenna • RF)

Portfolio: www.krishprasads.info/#projects

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Sunnyvale, CA, USA

US Visa : H1-B

EDUCATION

University of Texas at Dallas, USA

Master of Science in Electrical Engineering (RF & Microwave)

GPA: 3.77 / 4

Aug 2014 – Dec 2016

Courses: Antenna Design, Electromagnetics, RF Lab, RF Systems Engineering, RF Circuits, RFIC Design, RF Amplifier Design, Wireless Communications, Analog IC Design, Optical Communications, Digital Logic Design

Anna University, India

Bachelor of Engineering (Electrical & Electronics)

Percentage: 81%

Aug 2007 – May 2011

SKILLSET

- Software** : CST Microwave Studio, Keysight ADS Momentum, HFSS, xFDTD, AWR Microwave, Cadence Virtuoso & Allegro, Orcad Schematic editor & PCB Editor, NI Multisim
- Hardware** : Spectrum Analyzer, VNA, Anritsu MT8820C, R&S CMW-500, Power Meter, Oscilloscope, Anechoic chamber equipment, GTEM Compliance fixture, EM Scanner, Signal Generators
- Programming** : Python, Java, MATLAB, PHP, Visual Basic, Web Suite (HTML/CSS/JS)

RELEVANT EXPERIENCE

Google LLC, Hardware Designer (RF/Desense), Pixel Group

Nov 2019 – Present

- Designing consumer hardware products like 5G smartphones. Driving innovation through simulation driven design.

Amazon Lab 126, EMC/Desense & Antenna Design Engineer

Jan 2017 – Nov 2019

- Designed **echo**, **firetv**, **kindle** and **ring** products for best EMC & Desense from audio, display/touch, DDR, Camera and HDMI on Wi-Fi, BT, NFMI and WAN (LTE, WCDMA, GSM with AT&T and Vodafone) bands
- Designed LoRa, WiFi, BT product antennas and concept antennas to study best antenna-aggressor isolation
- Employed EM & circuit simulation tools to understand surface current patterns and coupling mechanisms to efficiently find practical and cost-effective fixes for best wireless performance
- Employed simulations for Desense and EMI problems to catch potential unintended radiators and apply fixes early in the program, saving hardware build and significant costs
- Debugged and solved EMI and Radiated second harmonic (RSE) compliance failures for multiple products
- Worked with Mechanical, Thermal, SW and Electrical engg teams in successful and timely release of products

Amazon Lab 126, Hardware Development Engineer Intern

May 2016 – Aug 2016

- Performed 3D EM (CST MWS) Simulations on PCB for aggressor-antenna isolation simulations and ADS for PSD estimations to establish Desense/Noise link budget
- Delivered on: ➤ Bring up of *EM Scanner setup with near field probes* for capturing radiated near fields
➤ Correlating Measured near fields with EM Scanner to Simulated current patterns from CST
- Trained on product dev process, Bench-level Desense debug via spectrum capture, Rate vs Range tests

Apple Inc., RF/OTA Systems Engineer Intern

Aug 2015 – Jan 2016

- Performed Active/Passive OTA tests in ETS/Satimo anechoic chambers using EM Quest and SatEnv
- Evaluated LTE & WCDMA (Signaling) performance of iPhone/iPads by Radiated(TRP/TIS) & Conducted Tests
- Obtained hands-on experience with R&S CMW 500, Spectrum Analyzer, VNA and Power Meter

Raman Research Institute, India, Research Intern

Mar 2013 – Mar 2014

- Worked in the end-to-end instrumentation of a Brain-Computer Interface System ([Presentation Link](#))
- Simulated & fabricated an EEG-Amplifier with analog filters and gain stages using NI MultiSim and Allegro

- Developed a Matched-Filter to study and identify voltage signatures emanating from Human Brain
- Developed a multi-channel analog signal sampler module (4 Channels @ 256 Hz)

Infosys Limited, India, Systems Engineer, Education & Research Dept **Aug 2011 – Jan 2013**

- Developed courseware and owned mid-level training on Java, Hadoop & MapReduce, Web Development
- Researched new technology prototypes and maintained critical internal projects

SSN Research Center, India, Research Intern **Jun 2010 – Aug 2010**

- Fabricated and characterized Silicon Nanowires by Vapor-Liquid-Solid Method using Plasma Enhanced Chemical Vapor Deposition (PECVD) process ([Presentation Link](#))
- Studied the impact of the presence of Silicon Nanowires on Photovoltaic Devices

PUBLICATIONS

Q. Huang, D. Pai, *Krishna Rao et. al*, "Accurate Prediction and Mitigation of EMI from high speed noise sources using full wave solver", IEEE EMC+SIPI 2019 Conference, New Orleans, LA, USA ([Link](#))

RELEVANT PROJECTS

Antenna/EMC/Desense/EM Portfolio – EM Simulations of antennas and mock PCBs ([Link](#))
 Hobbyist EM simulations for antennas (WiFi, BT, GPS), Waveguide filters and RFI/EMC concepts.

Antenna Design – Design & Test of a UWB (3GHz - 20GHz) Fractal Dipole Antenna ([Link](#))
 Modeled the structure in HFSS, analyzed VSWR, Current Distribution, Field Pattern. Studied the effects of varying microstrip feed geometry, fractal iteration count, port dimension sensitivity and manufacturing tolerances. Measured Return loss, Polarization and Far-field response (Co-pol and Cross-pol) with NSI scanner.

Microwave Design & Measurement Lab – Design & Measurements of passive RF circuits ([Link](#))
 Designed, simulated and characterized various RF Circuits like Resonators, Couplers, Power dividers, Patch Antenna, Filters, Mixers and Amplifiers. Simulation was performed using AWR MWO and EM simulation using AWR AXIEM. The circuits were later milled, ports and lumped elements soldered and tested to match the performance achieved in simulation. Soldering sizes up to 0402 were done.

Wireless Communications – Physical Layer Simulation of LTE-OFDM System ([Link](#))
 MATLAB based OFDM transmitter and receiver for a channel bandwidth of 3 MHz. Performance was compared for QPSK and 16-QAM modulation schemes for AWGN channel and multipath channel as well as indoor and outdoor channel models using the performance metric BER. Empirical spectral efficiency for models were plotted for a target BER of 10^{-3} when adaptive modulation was used.

RF Systems Engineering – RF System design for a Navigation & Comm system for a spacecraft ([Link](#))
 Designed and simulated a RADAR and Satellite-Communication system in AWR VSS. The spacecraft's communication system was designed to operate up to a distance of 450 million km, equipped with an onboard radar for debris avoidance. Simulations, Link Budget Analysis, Cascaded gain and Noise figure, P1DB, OIP3 calculations were manually calculated and verified using AWR-VSS.

RFIC Design – Design and layout of Q based Low noise amplifier in 2.4GHz band ([Link](#))
 Design, analysis and layout of an LNA with Gain > 12dB, IIP3 > -7dBm and NF < 2dB, including the effect of process and component variations. Using cascode stage to reduce Miller effect and to reduce the coupling between the output and input matching networks. Key parameters are formulated in terms of Q_{in} .